ADSP-21593/21594/ADSP-SC592/SC594 Processor Thermal Guidelines

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The ADSP-21593/21594/ADSP-SC592/SC594 processor is a dual-SHARC+® core DSP that doubles the audio performance of a single SHARC+ core and adds an integrated Arm Cortex-A5 core that runs up to 1 GHz. This high performance comes with an anticipated cost of increased power consumption and heat dissipation from the processor die. Issues related to heat dissipation and its mitigation is not new to any industry, but, could be considered as relatively newer to SHARC+ based applications. It is important to understand how to manage thermal analysis before designing a system and throughout the life cycle of the product.

This application note provides guidelines for evaluating thermal designs on systems using the ADSP-21593/21594/ADSP-SC592/SC594 family of processors. This document assumes that the reader is familiar with typical thermal design and management. The details shared in this document needs to be thoroughly evaluated and verified when applying to the actual system design. There are various standard, passive and active thermal management techniques such as heat sinks, fans, etc., that can be applied considering overall cost and mechanical requirements. Additionally, it is important to take into consideration the heat flow contributed by other components as well as any other system-level conditions.

Power Consumption

The power consumed by the chip is dissipated as thermal energy. If this heat is not dissipated fast enough, the chip temperature increases, and the junction temperature can cross beyond the maximum specification limit (125°C). Furthermore, this heat can also spread to other components on the board, if not evaluated and designed properly. In such cases, hot spots can occur in various regions of the board, and the temperature of other components can increase significantly.

The power consumption of the chip when running application software varies according to an increase in junction temperature. ADI provides a power calculator for ADSP-21593/21594/ADSP-SC592/SC594 processors[3]. Table 1 is extracted from the power calculator. For average power calculations, three typical application scenarios (activity levels) are considered; each scenario has different Activity Scaling Factor (ASF).

- Activity 1 - In this use case, all the accelerators (two FIR, four IIR) are assumed to be used 30% of time. All the cores are assumed to execute tight MAC operations 50% of time and IDLE operation 50% of time, on average.
- Activity 2 - In this use case, all the accelerators (two FIR, four IIR) are assumed to be used 50% of time. Both of the SHARC cores are assumed to execute tight MAC operations 70% of time and IDLE operation 30% of time , on average. The Arm core is assumed to execute 75% of time for tight math operations and 25% of time for IDLE operation, on average.

- Peak Activity - In this use case, all the accelerators are assumed to be used 70% of time. All of the cores are assumed to execute tight operations.

The following junction temperatures are considered:

- 85°C - Maximum junction temperature; typically used for consumer application.
- 100°C - High junction temperature used in automotive application.
- 125°C - Maximum junction temperature for the chip as well as for automotive applications

Activity Level	Junction Temperature for static power estimation (°C)	VDD_INT Dynamic Power (mW)	VDD_INT Static Power (mW)	Total VDD_INT Power (mW)
Activity 1	85	2433	859	3292
Activity 1	125	2423	2551	4974
Activity 2	100	2868	1293	4161
Activity 2	125	2868	2551	5419
Peak Activity	100	3301	1293	4594
Peak Activity	125	3301	2551	5852

Table 1: Power Calculations

Notes on Table 1:

- The power consumption of the activity levels are taken from the ADSP-SC59x power calculator [3]. Various clock frequencies are assumed to be the default values in the power calculator. Core clock is assumed to be 1GHz.
- Only power from VDD_INT at 1V is considered in thermal analysis. Power from other power supplies in the chip (VDD_EXT, VDD_REF, VDD_ANA, VDD_PLL, VDD_DMC) are not significant from a thermal perspective and, hence, are not considered.
- The ASF for each core and accelerators are mentioned, which contribute to the total power.
- The peak activity case is a worst-case software for the chip that is given only for reference. It will not be realistic in a customer use case.

The data in Table 1 illustrates how the VDD_INT power levels could vary with respect to the junction temperature of the processor die. For instance, there is an increase of 2W of static power, when the junction temperature rises from 85°C to 125°C between activity 1 and activity 2. Similarly, when we compare between activity 2 and peak activity, there is an increase of 1W when higher activity levels are executed at same temperature.

Phases of Thermal Analysis

The phases of thermal evaluation include thermal simulation of the system and the actual measurement on the board.

- During simulation, most of the inputs, including boundary conditions and the power consumption of the components, are derived out of estimations and overall system assumptions. Hence, the simulation results are highly dependent on the accuracy of these estimations.
- During the measurement phase, the total power, and temperature are measured physically to verify whether they are within limits by running end application software.

If the temperature dissipated by the processor and all other components in the system are well within their data sheet specification, then the thermal design may be taken forward. Otherwise, the assumptions taken during simulation may not have been accurate enough, and, hence, various board tests can be done to fine-tune simulation.

Thermal Simulation

Thermal simulation of a board uses 3D Computational Fluid Dynamics (CFD) software (FLOW-3D®). Flotherm® from Mentor Graphics (Siemens) and Icepack® from Ansys are popular tools in the market. There are many other vendors as well.

The ECXML Model

Electronics Cooling eXtensible Markup Language (ECXML) is a neutral file format intended to facilitate the provision of thermal models from suppliers to end users for use in 3D CFD thermal simulation tools. A de-facto standard for several years, ECXML is now published by JEDEC as the JEP181 guideline. Forcing a supplier to provide multiple proprietary formats that support these multiple tools is an onerous undertaking and one that, to date, has limited the availability of such simulation models. ECXML now published as JEDEC JEP181.

ADI provides an ECXML format package model for processors on the ADI website, its zip file[4] provides usage instructions. The instructions can be used with CFD thermal software that supports importing ECXML-based model.

There are several input parameters in a typical thermal simulation, as shown in Figure 1. ADI provides an estimation of the total power via the power calculator and provides the ECXML model of the package. The customer decides the ambient temperature. The details in the green box are also specific to the customer board and system. The important output of the simulation is the final junction temperature of the chip.

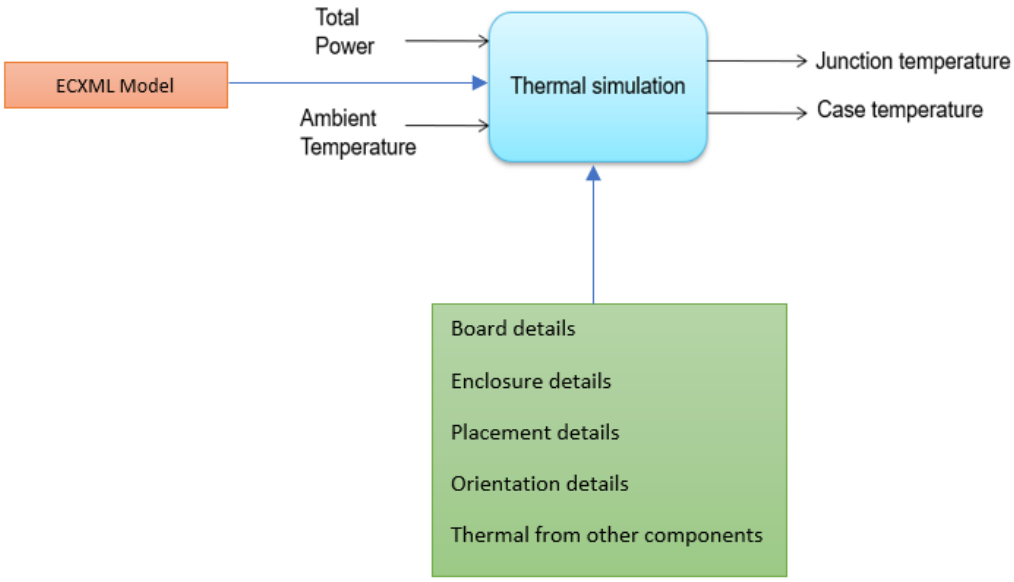

Figure 1:ECXML Inputs

The ECXML model is a package model with all material information including:

1. Thermal characteristics of the device
2. Dimensions of the package

Customers can use this model for their system-level thermal simulation.

Figure 2 is a pictural representation of the processor package (used only for reference). In the figure, the package size is 17mm x 17mm; the die size is 6.41mm x 5.42mm x 0.305um. All finer dimensions in the figure are available from the ECXML model.

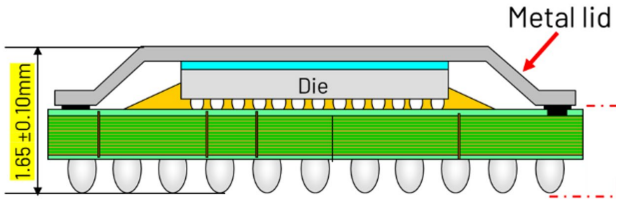

Figure 2: Reference Package

As mentioned in the processor data sheet, the application system thermal simulation is required for accurate temperature analysis. The thermal simulation must account for all specific 3D system design features, including, but not limited to other heat sources, use of heat sinks, use of thermal interface materials, and the system enclosure details. Thermal models of the package are available from Analog Devices product web page (under the Tools and Simulations tab). The thermal models are compatible with all major thermal simulation tools.

The use of JEDEC θJA, θJC, or ΨJT thermal parameters for application system thermal estimates is not recommended as indicated in the JEDEC51 specification[6]: "*This methodology is not meant to and will not predict the performance of a package in an application-specific environment*." Therefore, these parameters are no longer provided in the device data sheet.

Non-uniform power distribution

Legacy SHARC processor families such as ADSP-214xx as well as SHARC+ processor families such as ADSP-SC58x/ADSP-SC57x/ADSP-2156x products consume lower power (~2W to ~4W). The latest generation of products such as the ADSP-SC59x family consume higher power (>5W) owing to a greater number of high-performance cores and accelerators.

The higher power and larger silicon area results in non-uniform power distribution and subsequent hotspots. The ECXML model of the ADSP-21593/21594/ADSP-SC592/SC594 processor family considers uniform power distribution because it simplifies the thermal simulation. However, to account for these hotspots in simulation phase, an offset value must be added to the junction temperature obtained from simulations.

Different offset values across activity/power levels are provided in Table 2.

Activity Level	**Dynamic Power at 1V (mW)**	**Static Power at 125°C and 1V (mW)**	**Total Power at 1V (mW)**	**Offset (°C)**
Peak Activity	3301	2551	5852	6
Activity 2	2868	2551	5423	5
Activity 1	2433	2551	4984	4

Table 2: Offset Values

The offset values are provided for three different power-levels: peak activity, activity 2 and activity 1. The total power level should be mapped to one of the activity levels shown in the table. For power numbers which fall between two activity levels, choose the next higher activity. For example, if the simulation result from the ECXML mode is 110°C (Tj) and the total power is around 5200mW, then an offset of 6°C (from activity 2 level) must be added to 110°C. The final value from the simulation then becomes 116°C.

Static power influence on higher temperature – Simulation phase

Table 3 is a snapshot of the static current consumption from the power calculator.

Junction Temperature (°C)	Static Power (mW)
25	149.00
40	238.00
55	371.00
70	567.00
85	859.00
100	1293.00
105	1485.00
115	1951.00
125	2551.00

Table 3:Static Current Consumption

Table 3 shows that higher static current consumption is observed at higher junction temperatures. However, as discussed earlier, the thermal simulation can only consider ambient temperature and the total chip power consumption as input. The total chip power consumption (an input) depends on the junction temperature (an output). The following method can be used to account for this static power dependency on output junction temperature, during simulation.

- Method 1: Static power at maximum junction temperature (125°C) can be used as input (2551 mW). This covers worst case conditions, safely.
- Method 2: The thermal software must consider the input power as a function of output temperature; the final junction temperature is recorded after the simulation attains a steady saturated state. We expect customers to discuss the temperature influence on static current, with CFD software vendors. There may be various techniques in the software to ensure that rise in power with temperature is considered during simulation.

Since dynamic power does not increase significantly with temperature, it can be derived directly from power calculator and added to total power number.

Measuring Junction Temperature

The ADSP-21593/21594/ADSP-SC592/SC594 processors include a Thermal Monitoring Unit (TMU) module. The TMU is integrated into the processor die and digital infrastructure using an MMR-based system access to measure the die temperature variations in real-time. The TMU is a thermal sensor system that consists of temperature-sensors, a calibrated reference current source, and a current comparator. These sensors are placed strategically closer to various hot spots in the chip to allow software to read the maximum junction temperature recorded among multiple sensors.

The most important use case of the TMU is to let application know about whether the processor die temperature has crossed certain limits during run-time. These limits are configured as ALERT and FAULT limits during TMU initialization. The FAULT interrupt can be used to inform the external world that the chip temperature needs critical attention by various mechanism such as internal triggers or toggling a GPIO. For more information on the software programming of the TMU, refer to the hardware reference manual [2]. For information on the accuracy of the sensors in the TMU, refer to the device data sheet [1].

Sample Thermal Analysis

Thermal analysis including simulation were conducted on an internal bring up board (BUB) of the ADSP-21593 processor under different conditions (without a heatsink, with a heatsink and a thermal pad, and with a heatsink and thermal paste). Along with the processor, the board includes several interfaces such as Ethernet, DDR, RS232, Flash etc. and power supply components. There are no other high power components in the board.

These results are very specific to this board and cannot be used as it is on a different system or under different conditions. However, the intent of sharing these results is to illustrate two things:

- An emphasis on early thermal analysis that is required on these processors.
- To demonstrate a reference simulation and the corresponding board test results to demonstrate the correlation.

ADI recommends that customers perform careful system-level simulations to gain more accurate thermal results for their specific application. Table 4 shows the correlation achieved between actual physical test for a standalone evaluation board, thermal interface material and heatsink. Average correlation error for these tests is about 5 %. Note that there are no significant power-consuming components in this board, other than the processor. Additionally, no board enclosure is considered.

Ambient Temperature(°C)	Total Power (W)	Board Setup Details	Maximum Junction Temperature in Simulation (°C)	Maximum Junction Temperature in Testing (°C)
51	4.365	BUB board without heatsink	93	94
72	4.65	BUB with thermal pad (1mm, 3W/mK) and heat sink	113	109
72	4.664	BUB with heatsink with thermal paste (0.2mm, 1W/mk) and heat sink	112	109

Table 4: Sample Thermal Analysis

Recommendations for Thermal Relief

Since every system and hardware requirements are different, it is not possible to recommend specific reliefs. From the limited tests done on an evaluation board, the following observations were made:

- Thermal paste gives better results than thermal pads.
- Heat sinks may help in two situations: lower ambient temperature and/or lower current from the chip.
- Additional relief mechanisms such as controlled air-flow techniques (fan, coolant, etc.) may be required at higher temperatures, especially when there are several high-power components on the board.

Conclusion

Compared to older generation SHARC/SHARC+ processors, the ADSP-21593/21594/ADSP-SC592/SC594 processors can dissipate much more heat when running high performance audio applications. Specially at higher temperatures, it becomes challenging to control the heat dissipation without external measures such as heat sink or air flow. Early thermal analysis and design becomes important when operating the chip at higher temperature.

References

[1] *ADSP-21593/21594/ADSP-SC592/SC594 SHARC+ Dual Core DSP Data Sheet. Rev. D, August 2023*. Analog Devices, Inc.

[2] *ADSP-2159x /SC592/SC594 SHARC+ Processor Hardware Reference. Rev 0.6, May 2023*. Analog Devices, Inc.

[3] *EE-433: Estimating Power for ADSP-2159x/SC59x SHARC+ Processors. Rev. 1, April 2022.* Analog Devices, Inc. *https://www.analog.com/en/products/adsp-sc594.html#product-reference*

[4] Analog Devices, Inc. *Associated ZIP file. Thermal Models.* https://www.analog.com/media/en/simulation-models/compact-thermal-models/adsp-2159x-adsp-sc59x-fcbga-thermal-models.zip

[5] Bornoff, R. (2020, September 18). *What STEP was for CAD, ECXML is for electronics thermal simulation.* *https://blogs.sw.siemens.com/simcenter/ecxml-jedec-jep181-thermal/*

[6] *JEDEC. 2023. ECXML Guidelines for Electronic Thermal System Level Models – XML Requirements.* *https://www.jedec.org/standards-documents/docs/jep181*

Document History

Revision	Description
Rev 1 – September, 2023 by Prasanth Rajagopal, Deepak Huchaiah, Vikram Venkatadri	*Initial Release.*